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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,473	TRIVEDI, SUSHMA	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-66 are rejected under 35 U.S.C. 102(e) as being anticipated by Sazegari, U.S. Patent Number 6,446,198 (herein referred to as Sazegari).

4. Referring to claims 1 and 34 Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

receiving a string of bits;

generating a plurality of indices using a plurality of segments of bits in the string of bits (Sazegari abstract, figures 2-3, and 5, column 2 lines 17-43, column 3 lines 40-46, column 4 lines 5-46);

looking up simultaneously a plurality of entries from a plurality of look-up tables using the plurality of indices (Sazegari abstract, figures 2-3, and 5, column 2 lines 17-43, column 3 lines 40-46, column 4 lines 5-46; column 2 lines 17-25); and

combining the plurality of entries into a first result (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67);

wherein the above operations are performed in response to the microprocessor receiving the single instruction (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

5. Referring to claims 2 and 35 Sazegari has taught a method as in claim 1 further comprising:

receiving a plurality of data elements specifying the plurality of segments in the string of bits (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67; the 6^{th}-8^{th} bits show which results will be in the final result, and therefore what needs to be looked up with the indices).

6. Referring to claims 3 and 36 Sazegari has taught a method as in claim 2 wherein the plurality of data elements are received from an entry in a register file; and wherein the microprocessor is a media processor integrated with a memory controller on a single integrated circuit (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

7. Referring to claims 4 and 37 Sazegari has taught a method as in claim 3 wherein the single instruction specifies an index of the entry in the register file (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

8. Referring to claims 5 and 38 Sazegari has taught a method as in claim 2 further comprising:

receiving a bit pointer, wherein the plurality of segments in the string of bits are determined using the bit pointer and the plurality of data elements (Sazegari column 4 lines 63-67; the bits indicate which of the entries will be in the final result, in which they point to the entries making up the result).

9. Referring to claims 6 and 39 Sazegari has taught a method as in claim 5 further comprising:

generating a new bit pointer using the first result (Sazegari column 4 lines 63-67; the bits indicate which of the entries will be in the final result, in which they point to the entries making up the result, and there is a new set of bits pointing for each instruction).

10. Referring to claims 7 and 40 Sazegari has taught a method as in claim 1 further comprising:

receiving an offset, wherein the plurality of indices are determined using the offset and the plurality of segments of bits (Sazegari column 5 lines 1-20; shifting and offsetting are the same function).

11. Referring to claims 8 and 41 Sazegari has taught a method as in claim 1 further comprising:

partitioning look-up memory into the plurality of look-up tables before said looking-up (Sazegari column 2 lines 17-25);

wherein the microprocessor is a media processor formed on a monolithic integrated circuit .

12. Referring to claims 9 and 42 Sazegari has taught a method as in claim 8 wherein the look-up memory comprises a plurality of look-up units, and wherein said partitioning look-up memory comprises:

configuring the plurality of look-up units into the plurality of look-up tables (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25).

13. Referring to claims 10 and 43 Sazegari has taught a method as in claim 23 wherein each of the plurality of look-up units comprises 256 8-bit entries (Sazegari column 3 lines 57-58, column 2 lines 35-43).

14. Referring to claims 11 and 44 Sazegari has taught a method as in claim 1 wherein the single instruction specifies a total number of entries contained in each of the plurality of look-up tables (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25.

15. Referring to claims 12 and 45 Sazegari has taught a method as in claim 11 wherein the total number of entries is one of:

a) 256 (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25);

b) 512; and

c) 1024.

16. Referring to claims 13 and 46 Sazegari has taught a method as in claim 1 wherein the single instruction specifies a total number of bits used by each entry contained in the plurality of look-up tables (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25).

17. Referring to claims 14 and 47 Sazegari has taught a method as in claim 13 wherein the total number of bits is one of:

a) 8 (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25);

b) 16; and

c) 24.

18. Referring to claims 15 and 48 Sazegari has taught a method as in claim 8 wherein the plurality of look-up tables are configure according to an indicator in an entry in a register file (Sazegari column 3 lines 57-58, column 2 lines 35-43, column 2 lines 17-25).

19. Referring to claims 16 and 49 Sazegari has taught a method as in claim 15 wherein the single instruction specifies an index of the entry in the register file (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

20. Referring to claims 17 and 50 Sazegari has taught a method as in claim 1 wherein said combining the plurality of entries comprises:

selecting a valid data from the plurality of entries (Sazegari column 4 lines 63-67; the bits indicate which of the entries will be in the final result, which makes them valid, otherwise they are not in the final result).

21. Referring to claims 18 and 51 Sazegari has taught a method as in claim 17 further comprising:

generating an indicator indicating whether none of the plurality of entries is valid (Sazegari column 4 lines 63-67; the bits indicate which of the entries will be in the final result, which makes them valid, otherwise they are not in the final result).

22. Referring to claims 19 and 52 Sazegari has taught a method as in claim 17 wherein the valid data is selected according to priorities of the look-up tables from which the plurality of entries are looked UP (Sazegari column 4 lines 63-67; the bits indicate which of the entries will be in the final result, which makes them valid, otherwise they are not in the final result).

23. Referring to claims 20 and 53 Sazegari has taught a method as in claim 17 wherein said combining the plurality of entries further comprises:

formatting the valid data according to a type of the valid data (Sazegari column 4 lines 63-67; the bits indicate which of the entries will be in the final result, which makes them valid, otherwise they are not in the final result).

24. Referring to claims 21 and 54 Sazegari has taught a method as in claim 20 wherein the type of the valid data is one of:

a) zero fill;

b) sign magnitude; and

c) two complement (Sazegari column 3 lines 24-36; the processor described uses a two complement format).

25. Referring to claims 22 and 55 Sazegari has taught a method as in claim 21 further comprising:

retrieving a sign bit from the string of bits for the valid data, wherein the first result is obtained by formatting the valid data using the sign bit when the type of the valid data is sign magnitude (Sazegari column 4 lines 63-67; the bits indicate which of the entries will be in the final result, which makes them valid, otherwise they are not in the final result).

26. Referring to claims 23 and 56 Sazegari has taught a method as in claim 1 wherein an entry in the plurality of entries contains:

a) information indicating whether the entry is valid (Sazegari column 4 lines 63-67; the bits indicate which of the entries will be in the final result, which makes them valid, otherwise they are not in the final result);

b) information indicating a type of the entry; and

c) information indicating a number of bits of a code word to be decoded.

27. Referring to claims 24 and 57 Sazegari has taught a method as in claim 1 wherein the string is received from an entry in a register file (Sazegari Figure 2 column 3 line 64-column 4 line 4).

28. Referring to claims 25 and 58 Sazegari has taught a method as in claim 24 wherein the single instruction specifies an index of the entry in the register file (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

29. Referring to claims 26 and 59 Sazegari has taught a method as in claim 1 further comprising:

receiving a first number indicating a position of a last bit of input in the string of bit (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

30. Referring to claims 27 and 60 Sazegari has taught a method as in claim 26 further comprising:

generating an indicator indicating whether any bit after the last bit of input is used in obtaining the first result (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

31. Referring to claims 28 and 61 Sazegari has taught a method as in claim 12 further comprising:

generating an indicator indicating whether one of the plurality of segments of bits contains a predetermined code (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

32. Referring to claims 29 and 62 Sazegari has taught a method as in claim 28 wherein the predetermined code represents an end of block condition (Sazegari abstract, figures 2-3, and 5, column 4 lines 5-67).

33. Referring to claims 30 and 63 Sazegari has taught a method as in claim 1 further composing:

receiving at least one format;

formatting the string of bits into at least one escape data according to the at least one format; and

combining the at least one escape data and the first result into a second result (Sazegari abstract, figures 2-3, and 5, column 2 lines 17-43, column 3 lines 40-46, column 4 lines 5-46; column 2 lines 17-25).

34. Referring to claims 31 and 64 Sazegari has taught a method as in claim 30 wherein one of the at least one format is for data of a type which is one of:

a) zero fill;

b) sign magnitude; and

c) two complement (Sazegari column 3 lines 24-36; the processor described uses a two complement format).

35. Referring to claims 32 and 65 Sazegari has taught a method as in claim 30 wherein the at least one format is received from an entry of a register file (Sazegari abstract, figures 2-3, and 5, column 2 lines 17-43, column 3 lines 40-46, column 4 lines 5-46; column 2 lines 17-25).

36. Referring to claims 33 and 66 Sazegari has taught a method as in claim 32 wherein the single instruction specifies an index of the entry in the register file (Sazegari abstract, figures 2-

3, and 5, column 2 lines 17-43, column 3 lines 40-46, column 4 lines 5-46; column 2 lines 17-25).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

> Scales et al., U.S. Patent Number 6,334,176, has taught a method for aligning instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 571-272-4167. The examiner can normally be reached on 9Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Harkness

Examiner

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December 8, 2004